WHAT IS CLAIMED IS:

1. A system for reducing power consumption in digital circuits using charge redistribution, comprising:

- a plurality of signal lines;
- an intermediate floating virtual source/sink, and

a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source/sink during an idle period prior to a change of state.

2. The system as claimed in claim 1 wherein the intermediate floating virtual source/sink comprises a charge storage element.

3. The system as claimed in claim 1 wherein the charge redistribution circuit comprising the transition detector connected to the signal line having two outputs, one of which is connected to the input of a tri-state driver circuit and the other output simultaneously disable the tri-state driver circuit, and enables the control switch to connect its output to the floating source/sink whenever a transition is detected on a signal line.

4. The system as claimed in claim 2 wherein the charge storage element is a capacitor or a set of capacitors.

5. The system as claimed in claim 3 wherein the transition detector comprising a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detector and to the first input of a 2-input exclusive-OR or exclusive-NOR gate while the second input of the exclusive-OR/ exclusive-NOR gate is directly connected to the signal line and its output is connected to the second output of the Transition Detector.

6. The system as claimed in claim 4 wherein the capacitor comprising a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

7. An integrated circuit for reducing power consumption in digital circuits using charge redistribution, comprising:

a plurality of signal lines;

an intermediate floating virtual source/sink, and

a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source/sink during an idle period prior to a change of state.

8. An integrated circuit as claimed in claim 7 wherein the intermediate floating virtual source/sink comprises a charge storage element.

9. An integrated circuit as claimed in claim 7 wherein the charge redistribution circuit comprising the transition detector connected to the signal line having two outputs, one of which is connected to the input of a tri-state driver circuit and the other output simultaneously disable the tri-state driver circuit and enables the control switch to connect its output to the floating source/sink whenever a transition is detected on a signal line.

10. An integrated circuit as claimed in claim 8 wherein the charge storage element is a capacitor or a set of capacitors.

11. An integrated circuit as claimed in claim 9 wherein the transition detector comprising a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detects and to the first input of a 2-input exclusive-OR or exclusive-NOR gate while the second input of the exclusive-OR/ exclusive-NOR fate is directly connected to the signal line, its output is connected to the second output of the Transition Detector.

12. An integrated circuit as claimed in claim 10 wherein the capacitor comprises a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

13. A method for reducing power consumption in digital circuits using charge redistribution, comprising the steps of:

providing a plurality of signal lines;

providing an intermediate floating virtual source/sink, and

isolating each signal line from its source circuit and connecting it to the intermediate floating virtual source/sink during an idle period prior to a change of state.

14. The method as claimed in claim 13 wherein the step of providing an intermediate floating virtual source/sink comprising supplying a charge storage element.

15. The method as claimed in claim 13 wherein the change of state is identified by detecting a transition on the signal line.

16. The method as claimed in claim 14 wherein the charge storage element is supplied by connecting a capacitor or a set of capacitors.

17. The method as claimed in claim 15 wherein the transition is detected by exclusive-NORing or exclusive-ORing the signal with a delayed version of the signal.

18. The method as claimed in claim 15 wherein the signal line is connected to the intermediate floating virtual source/sink whenever a transition is detected.

19. The method as claimed in claim 16 wherein the capacitor is provided by a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.